AH741C

Two-wire differential wheel speed sensor

1. Product Introduction

AH741C is a new-generation wheel speed sensor chip developed by Alfa Electronics Co. Ltd based on advanced differential Hall technology and high-performance, dedicated ASIC signal processor. The chip is mainly used in modern vehicle power control system ABS to provide speed information, and the output is a two-wire current interface. The sensor operates without external components and combines fast power-on times with low cutoff frequencies, excellent accuracy and sensitivity for demanding automotive requirements such as wide temperature ranges, high ESD and EMC robustness.

Finally, optimized piezoelectric compensation and integrated dynamic offset compensation improve the sensor's immunity to any unwanted stray magnetic field, ferromagnetic particles or other disturbances.

The AH741C also offers an integrated 1.8 nF capacitor for improved EMI performance.

2. Product Features

- Two-wire current interface
- Dynamic self-calibration principle
- single chip solution
- No external components are required
- High sensitivity
- Back magnetic north and south pole self-induction
- High resistance piezoelectric effect
- Large working air gap
- Wide operating temperature range
- PG-SSO-2-4 package, RoHS certified

3. Application

- Anti-lock Braking System (ABS)
- Electronic Stability System (ESP)
- Automatic transmission
- Wheel speed sensing in automotive applications

Table of Contents

4. Product packaging

Part No.	operation temperature	Packages	Packing
AH741	-40℃~150℃	PG-SSO-2-4	Braid, 1500 pieces/box
AH741C	-40℃~150℃	PG-SSO-2-4	Braid, 1500 pieces/box

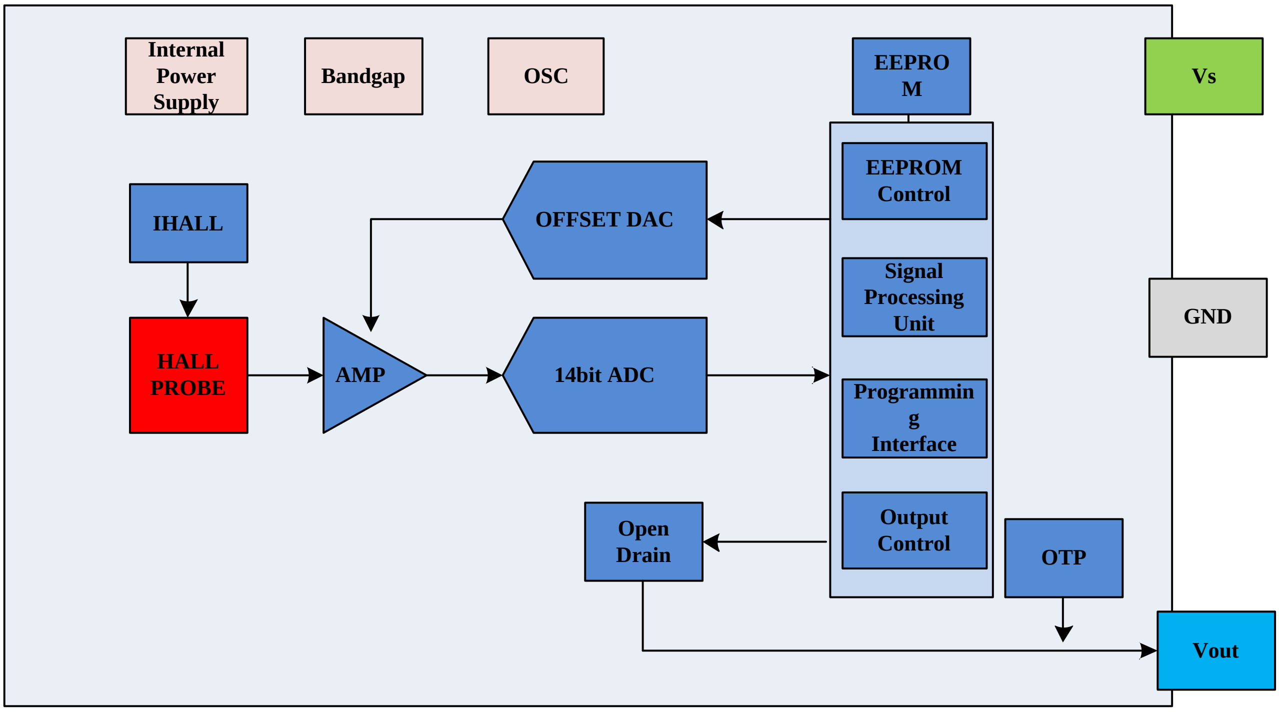
5. Naming convention

Part number AH741----C

① ②

①Series name ②C means built-in 1.8nF capacitor

6. Functional Block Diagram



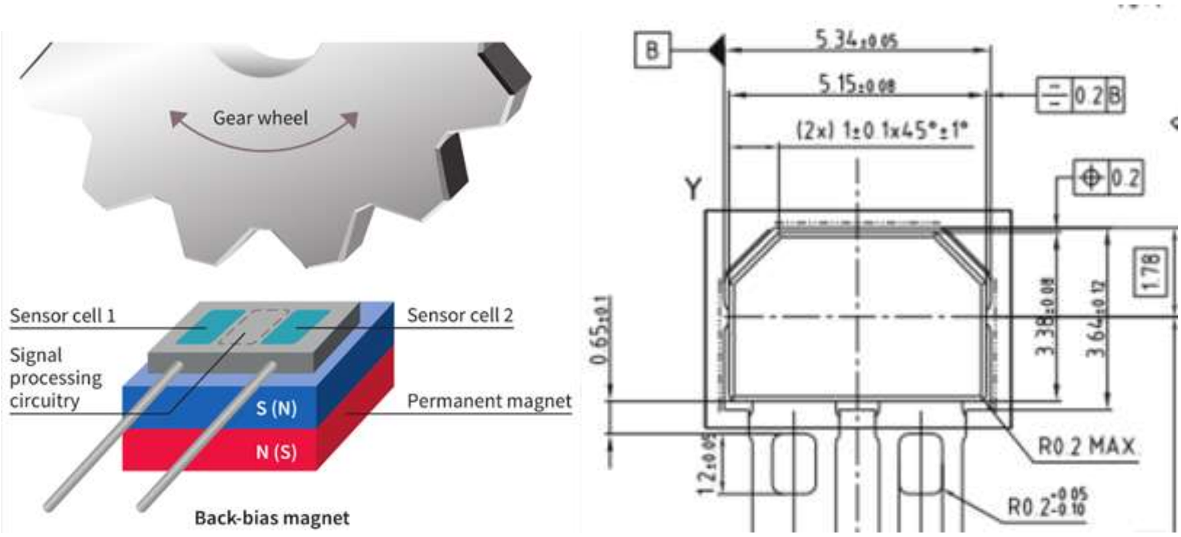
6-1: Functional block diagram

The circuit is powered internally by a 3v voltage regulator, and an oscillator on the chip acts as a clock generator for the digital part of the circuit. The AH741C signal path consists of a pair of Hall probes spaced 2.5mm apart, a differential amplifier, a noise limiting low-pass filter, and a comparator that powers the switching current output stage. In addition, there are signal tracking A/D converters, digital signal processors (DSP) and offset D/A converters to provide offset feedback loops.

During startup (not calibrated mode), output is disabled ($I=I_{LOW}$). The differential input signal is digitized in a high-speed A/D converter and fed into the DSP. The minimum and maximum values of the input signal are extracted and their corresponding arithmetic mean values are calculated, the offset of which is determined and the offset offset DAC is fed.

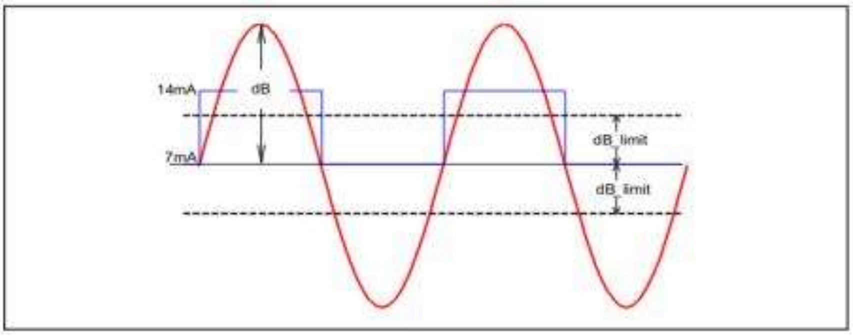
After correcting the offset successfully, turn on the output switch. In the running mode (calibration mode), the DSP bias correction algorithm switches to the low jitter mode, avoiding the oscillation of the biased DAC LSB. The switch occurs at zero crossing. It is only affected by the (small) residual offset of the comparator and the residual propagation delay time of the signal path, which is mainly determined by the noise limiting filter, and signals below the defined threshold dB_{Limit} (Figure 6-3) are not detected to avoid unnecessary parasitic switching.

In general, differential Hall sensor IC measure the differential flux density of magnetic fields by detecting the motion of ferromagnetic and permanent magnet structures. The magnetic field that detects the motion of a ferromagnetic object, such as a gear, is provided by a back permanent magnet with the north or South Pole of the magnet attached to the back of the IC package (Figure 6-2).



6-2 Sensor installation and sensing position

Magnetic offsets up to ±20mT are eliminated by a self-calibration algorithm, with only a few magnetic edges necessary for self-calibration. After the bias calibration sequence, the switch occurs when the input signal crosses the arithmetic mean of its maximum value, the minimum value (such as zero crossing of the sine signal), the on and off state of the IC is indicated by the high and low current consumption, as shown in Figure 6-3 when the difference field dB>0, the output high current IHIGH(14mA); When the difference field dB<0, the output low current ILOW(7mA).

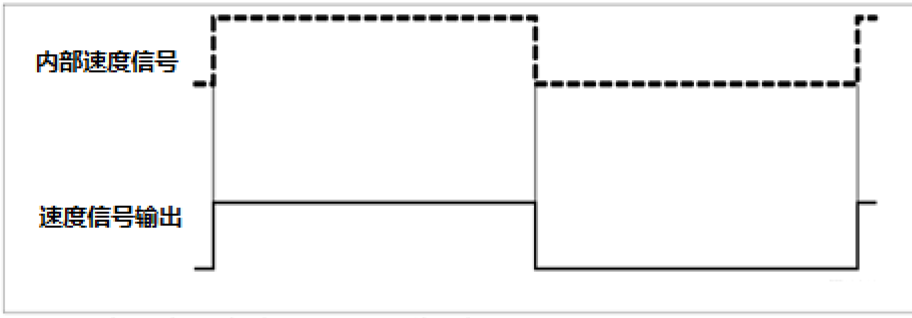


6-3 Differential magnetic field dB and switching threshold dBlimit (calibration mode)

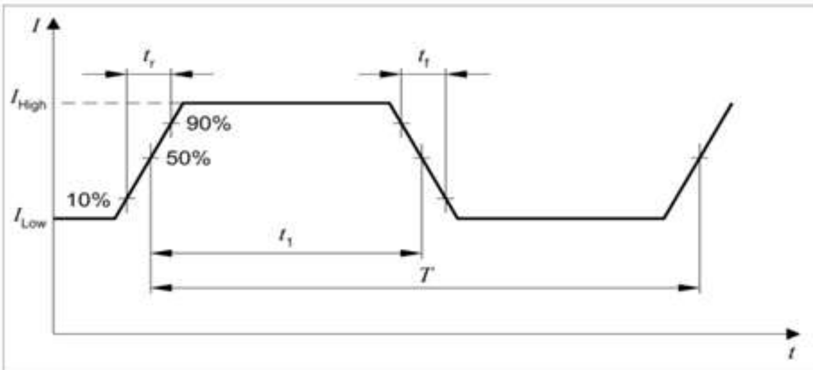
Note: dB is the resulting signal of the difference between the left and right Hall components (right - left). Here dB = b2(right)- b1(left) .

7. Output description

Under ideal conditions, the output shows a duty cycle of 50%. Under real conditions, the duty cycle is determined by the mechanical size of the target wheel and its tolerance (due to the principle of zero crossing, the spacing >4mm May exceed 40% to 60%).

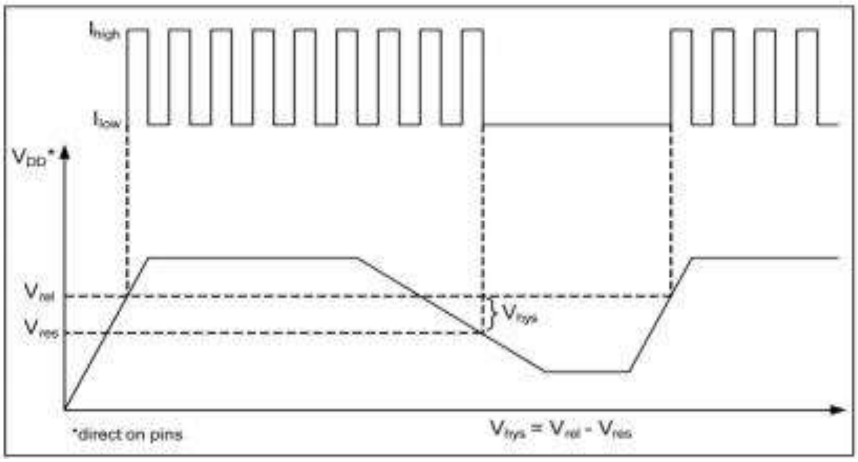


7- 1 Speed signal (frequency is speed)



7-2 Signal Signal rising tr, falling tf time definition, period, duty cycle definition DC= t 1 /T x 100%

For low voltage behavior, the voltage supply comparator has an integrated hysteresis Vhys whose release level Vrel has a maximum value < 4.5V. This determines the minimum power supply voltage V_{DD} required for the chip. The minimum hysteresis is achieved at 0.7V, thus avoiding the additional voltage drop at RM (designed for RM=75Ω) when the supply voltage VDD is switched from a low current level to a high current level and V_{DD} =4.5V.



7-3 Startup and undervoltage waveforms

8. Absolute limit parameter

The absolute maximum rating is the limit value that the chip can withstand, beyond which the chip may be permanently damaged.

Parameter	Symbol	Min	Max	Unit	Condition
Power supply Voltage	V_{DD}	-0.3	-	V	T_j<80℃
		-	20	V	T_j=150℃,t=10×5min.
		-	24	V	R_M≥75Ωincluded in V_{DD},t=10×5min.
		-	27	V	t=400ms,R_M≥75Ω,included in VDD
Reverse voltage	U_{rev}	-22		V	R_M≥75Ω included in V_{DD},t<1h
Reverse polarity current	I_{rev}	-	200	mA	External current limitation required, t < 4 h
			300	mA	External current limitation required, t < 1 h
Operating ambient temperature	T_A	-40	150	℃	-
Antistatic capacity	V_{ESD}		±12	KV	AEC-Q100

9. Electrical characteristic

Unless otherwise specified, the following parameters are tested under constant amplitude and bias of the input signal (test conditions are V_{DD}=12V, T_A=25℃, circuit reference test circuit Figure 12- 1).

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Electrical characteristic						
Operating voltage	V_{DD}	4.5	-	27	V	
Operating current (low)	I_{LOW}	5.9	7	8.4	mA	
Working current (high)	I_{HIGH}	11.8	14	16.8	mA	
Working current ratio	I_{HIGH}/I_{LOW}	1.9	2.1	2.3		
Output swing rate	t_r(rise)	8		22	mA/μs	R_M = 75 Ω +/-5% Tj<125°C
	t_f(down)	8		28	mA/μs	R_M = 75 Ω +/-5% Tj<170°C
linearity	dI/dV_{DD}			90	μA/V	
Initial calibration delay	$t_{d,input}$		120	300	μs	
Power-on time u	t_{pu}			100	μs	
Duty cycle	DC	40	50	60	%	
Signal frequency	f	1		2500	Hz	
		2500		10000	Hz	
Signal Jitter Tj<150°C Tj<170°C 1Hz<f<2500Hz	$S_{Jit\text{-}close}$			±2 ±3	%	1σ value VDD = 12 V ΔB ≥ 2 mT
Signal Jitter Tj<150°C Tj<170°C 2500 Hz < f < 10000 Hz	$S_{Jit\text{-}close}$			±3 ±4.5	%	1σ value VDD = 12 V ΔB ≥ 2 mT

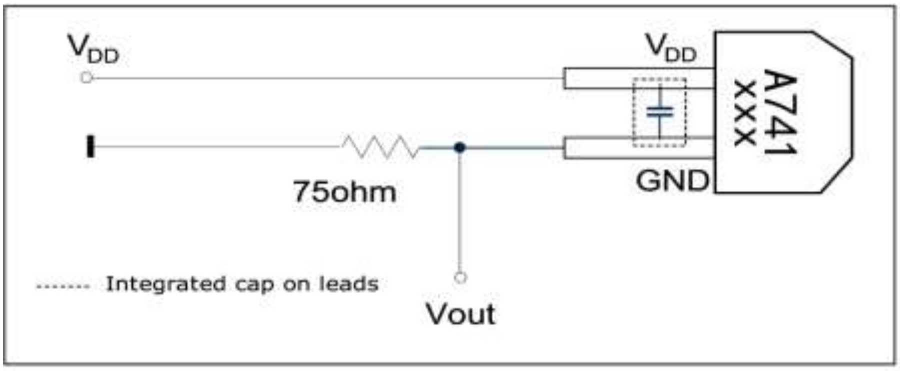
10. Magnetic field characteristic

Unless otherwise specified, the following parameters are tested under constant amplitude and bias of the input signal (test conditions are V_{DD}=12V, T_A=25°C, circuit reference test circuit Figure 12- 1).

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Pre-induction	B_0	-500	-	+500	mT	

Pre-induction offset between outer probes	$\Delta B_{stat., l/r}$	-30		+30	mT	
Differential induction	ΔB	-120		+120	mT	f=1kHz, Bdiff=5mT
Threshold limit	ΔB_{Limit}	0.35	0.7	1.5	mT	$1Hz<f_{mag}<2500Hz$
				1.7	mT	$2500Hz<f_{mag}<10000Hz$
The difference in the magnetic field required to start	$\Delta B_{startup}$	0.7	1.4	3.3	mT	$1Hz<f_{mag}<2500Hz$
				3.9	mT	$2500Hz<f_{mag}<10000Hz$

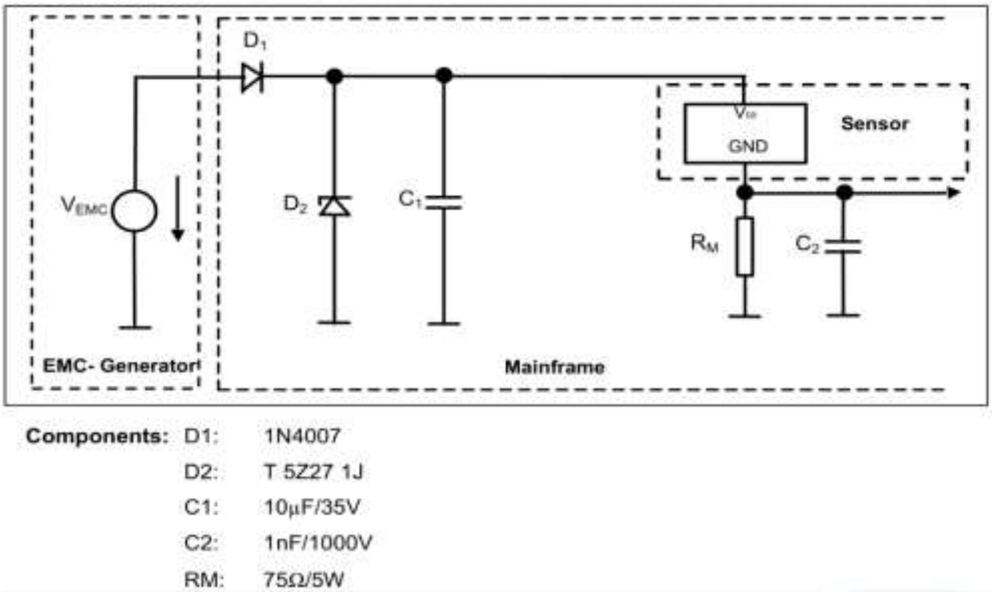
11. Test circuit



11-1 Test circuit

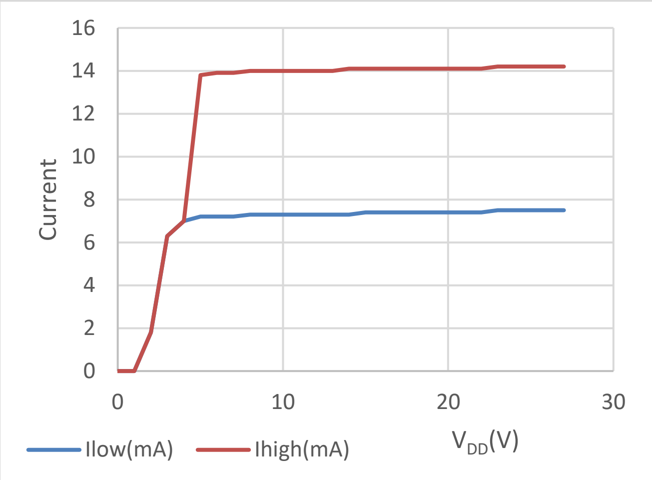
12. Reference circuit

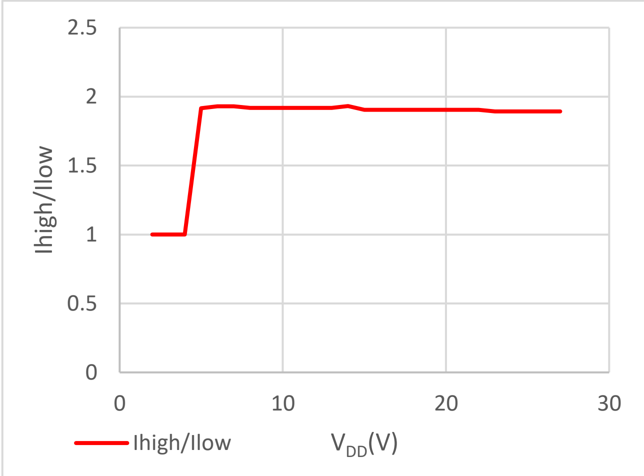
Application reference circuit



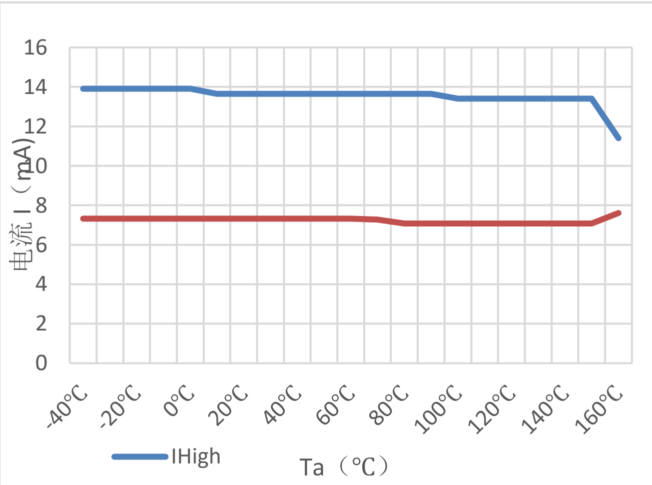
12- 1 Application reference circuit

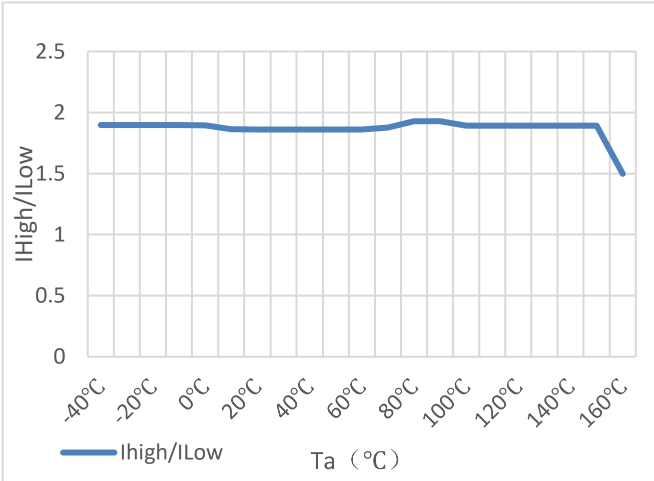
13. Characteristic curve



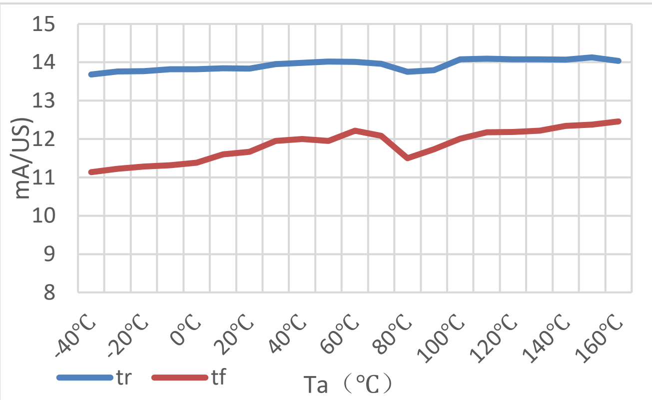


13- 1 Operating current and current ratio at a voltage of 0 to 28V

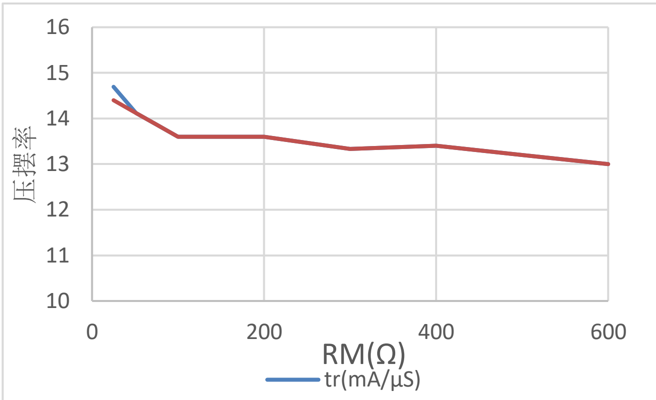




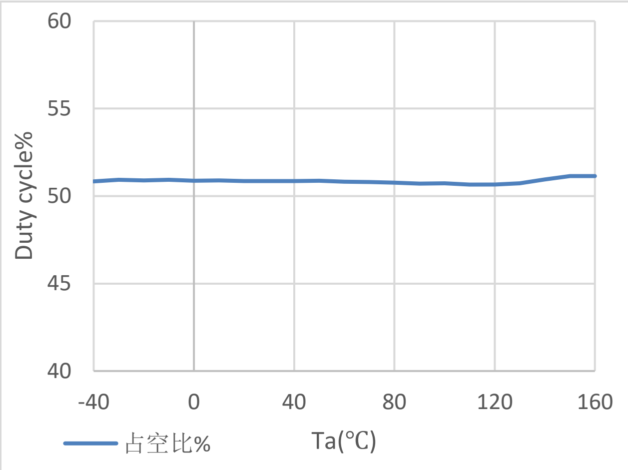
13-2 -40 to +150 °C Operating current and current ratio

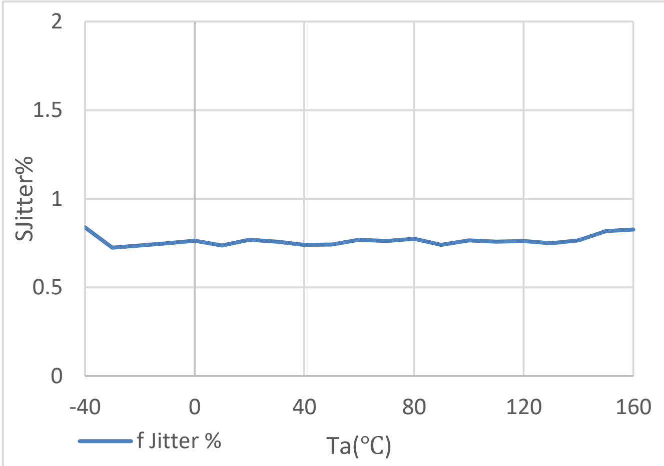


13-3 Output signal slew rate at -40~+150 °C temperature



13-4 RM (1~600 Ω) output signal slew rate

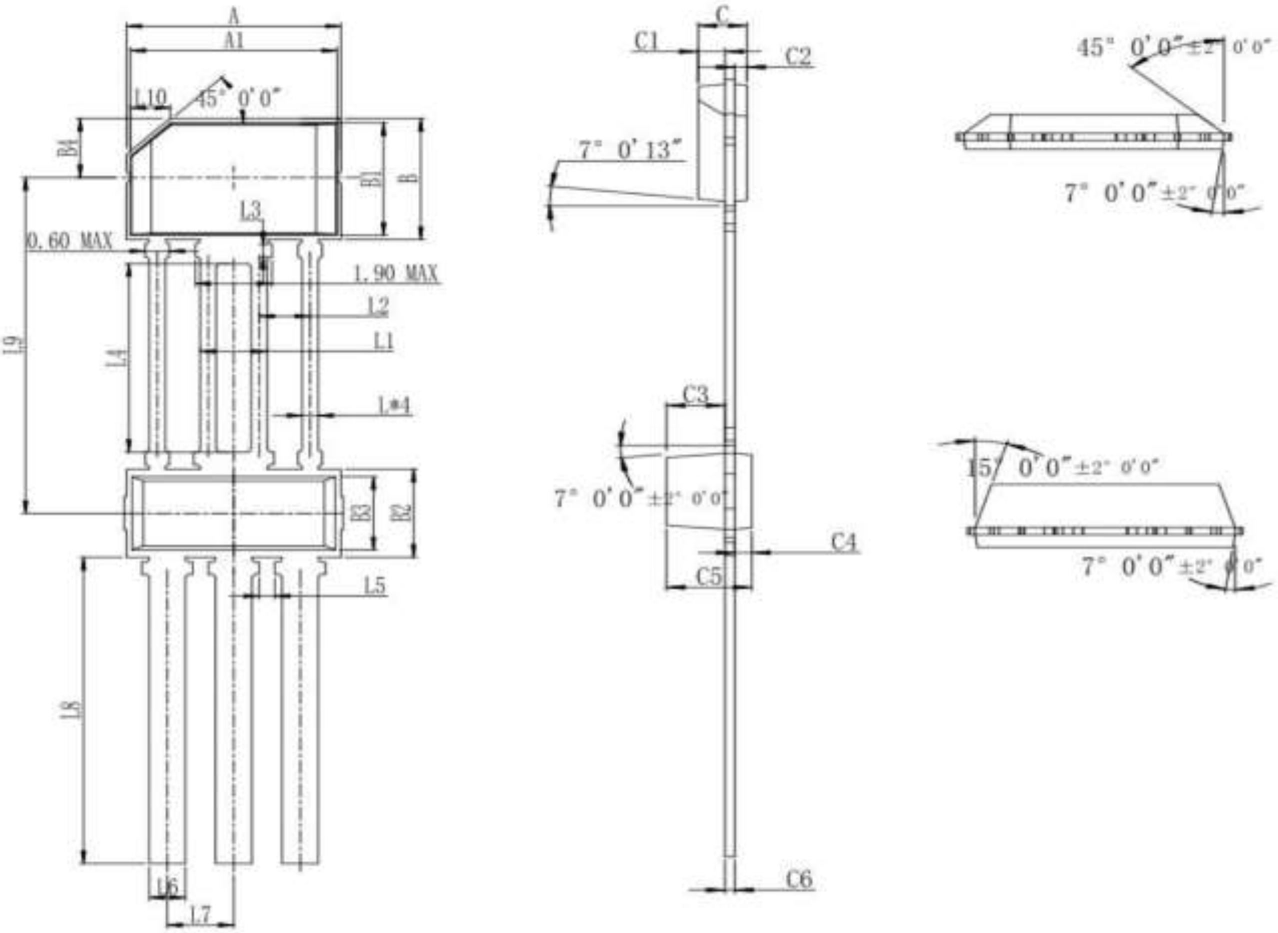




13-5 Output signal duty cycle at -40 to 150 °C temperature

13-6 Output signal frequency jitter at -40 to 150 °C temperature

14. Package information



15.Note

- Hall chips are sensitive devices, and electrostatic protection measures should be taken during use, installation, and storage.
- During installation and use, mechanical stress applied to the device casing and leads should be minimized as much as possible.
- It is recommended that the welding temperature should not exceed 350 ℃ and the duration should not exceed 5 seconds.
- To ensure the safety and stability of Hall chips, it is not recommended to use them beyond the parameter range for a long time.

16. Historical Version

No.	Time	Describe
1	May,2024	Compile and update some ambiguous text descriptions
2	December,2024	Update TO94-3 package
3	April,2025	Update the encapsulation type and add PG-SSO-3-52 encapsulation