AH742C

Two-wire differential wheel speed sensor (speed direction)

Alfa Electronics Co.,Ltd

1. Product Introduction

AH742C is a new generation wheel speed and direction detection sensor chip developed by Alfa Electronics Co. Ltd based on advanced differential Hall technology and high-performance, dedicated ASIC signal processor. This chip is mainly used in the modern vehicle power control system ABS to provide information on speed and rotation direction, assembly position, and limited air gap. The output is a two-wire current interface based on pulse width modulation (PWM) principle. This sensor does not require external components to operate and combines fast power on time with low cutoff frequency. Its excellent accuracy and sensitivity are suitable for demanding automotive requirements such as wide temperature range, high ESD, and EMC robustness.

Optimized piezoelectric compensation and integrated dynamic offset compensation improve the sensor's anti-interference ability against stray magnetic fields, ferromagnetic particles, or other disturbances.

AH742C also offers an external 1.8nF capacitor to enhance EMC performance.

2. Product Features

- Two wire PWM current output interface
- Rotation direction detection
- Air gap diagnosis
- Assembly position diagnosis
- Dynamic automatic calibration
- Single chip solution, no need for external components
- High sensitivity
- Back magnetic north and south pole self induction
- High resistance piezoelectric effect
- Large working air gap
- Wide working temperature rang
- PG-SSO-2-4 package, RoHS certified

3. Application

- Anti-lock Braking System (ABS)
- Electronic Stability System (ESP)
- Automatic transmission
- Wheel speed sensing in automotive applications
- Other similar fields of wheel speed detection

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4. Product packaging

Part No.	operation temperature	Packages	Packing
AH742C	-40℃~150℃	PG-SSO-2-4	Braid, 1500 pieces/box

5. Naming convention

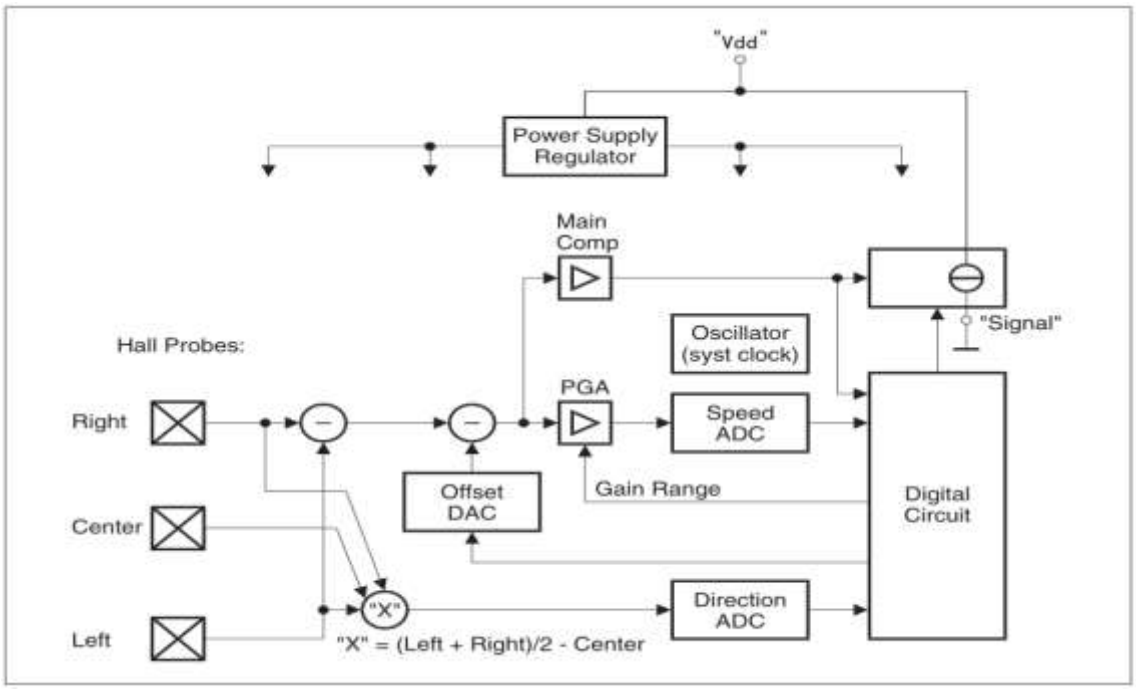
Part number AH742----C

① ②

①Series name ②C means built-in 1.8nF capacitor

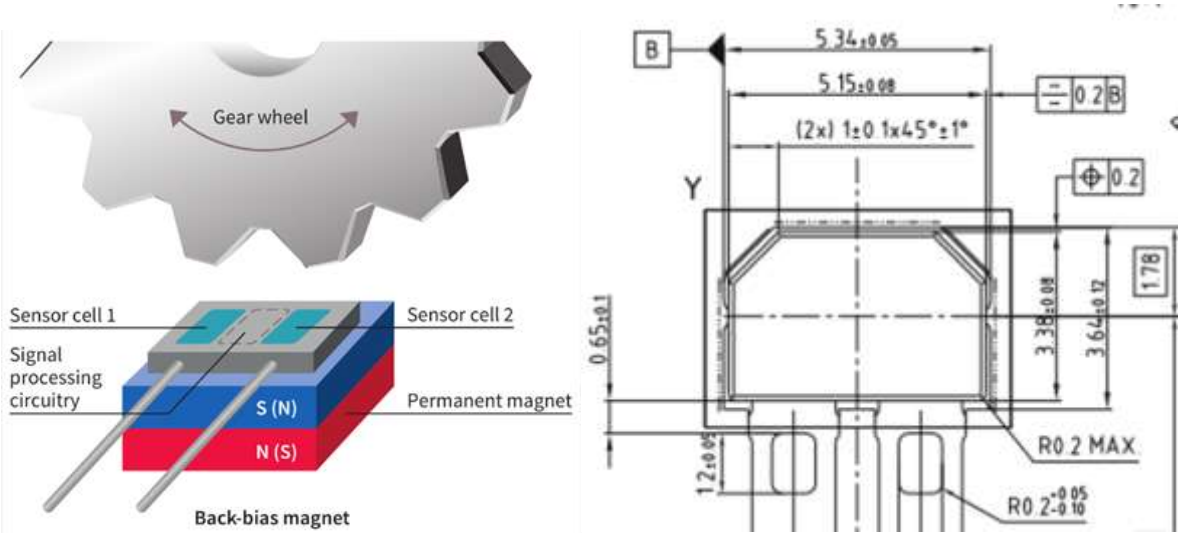
6. Function Description

The AH742C circuit is powered internally by a 3V voltage regulator, and the on-chip oscillator serves as the clock generator for the DSP and output encoder. The AH742C signal path consists of a pair of Hall effect probes spaced 2.5mm apart, a differential amplifier with a noise limiting low-pass filter, and a comparator with a trigger switch current output stage. In addition, there are speed signal, direction signal tracking A/D converters, digital signal processors (DSPs), and offset cancellation D/A converters that provide offset cancellation feedback loops, as shown in Figure 6-1.



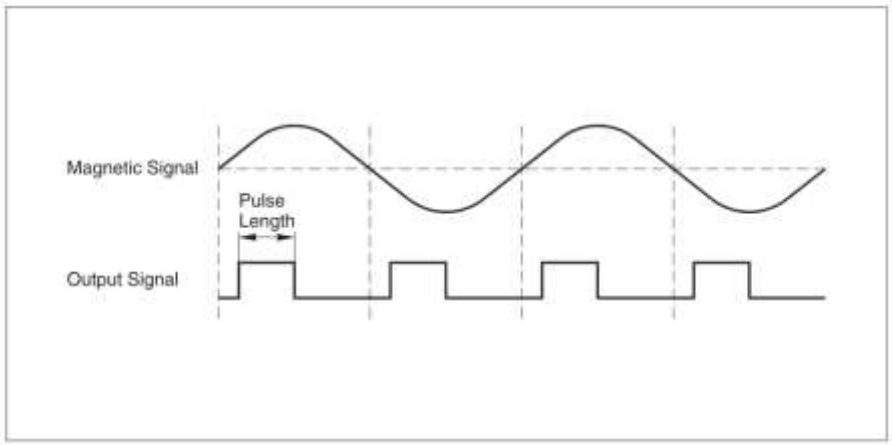
6-1: Functional block diagram

Differential Hall effect integrated circuits detect the motion of ferromagnetic or permanent magnetic structures by measuring the differential magnetic flux density of the magnetic field. In order to detect the motion of ferromagnetic objects, the magnetic field for detecting the motion of ferromagnetic objects (such as gears) must be provided by a back biased permanent magnet. The south or north pole of the magnet can be attached to the back of the IC package, on the unmarked side, as shown in Figure 6-2.



6-2 Sensor installation and sensing position

Magnetic offsets up to ±20mT are eliminated by a self-calibration algorithm, the self calibration process can be completed with only a few conversions. After initial self calibration, when the input signal exceeds the arithmetic mean of its maximum and minimum values (such as the zero crossing of a sine signal), the sequence switches. The on/off status of the IC is indicated by high and low current consumption. Each zero crossing of the magnetic input signal triggers an output pulse, as shown in Figure 6-3. During the power on phase, the output is disabled (low state).



6-3 Zero crossing principle and corresponding pulse output

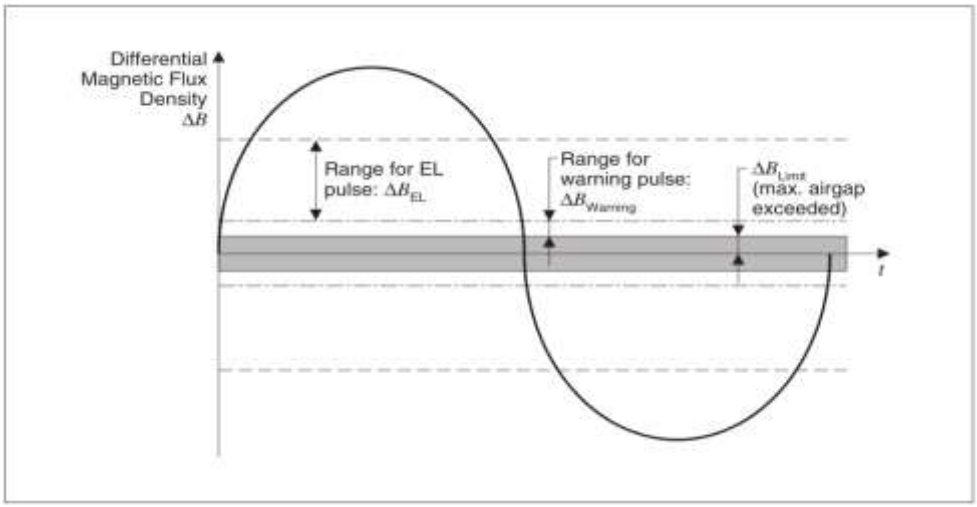
In addition to the speed signal, changing the length of the output pulse (PWM modulation) in Figure 6-3 can also provide the following information:

1) Air gap warning range Warning

When the magnetic field is below the critical value (such as when the air gap between the Hall effect IC and the target wheel exceeds the critical value), as shown in Figure 6-4. The output pulse length will issue a warning message. The functionality of the chip is limited, and warning messages are only given in calibration mode. The warning pulse length is 45 μ s.

2) Assembly position range EL

When the magnetic field is lower than the predetermined value (the air gap between the Hall effect IC and the target wheel exceeds the predetermined value), as shown in Figure 4-4. Send EL information in the output pulse length. The chip has all functions. The pulse length is 360 μ s when turning left and 720 μ s when turning right.



6-4 Definition of Differential Magnetic Field Flux Density Range

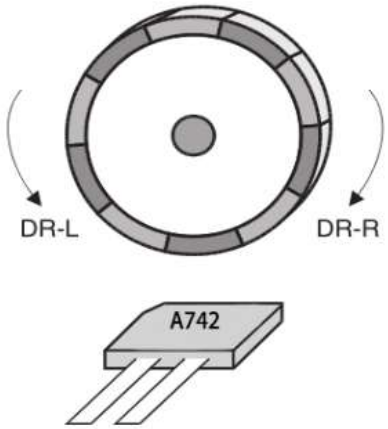
3) Rotate direction DR-R to the right

When the target wheel Hall chip moves from the right pin (GND) to the left pin (VDD), the output pulse length emits DR-R information, as shown in Figure 4-5. When turning right, the pulse length is 180 μ s or 720 μ s.

4) Left rotation direction DR-L

When the target wheel moves from the VDD pin to the GND pin above the Hall chip, the output pulse length will emit DR-L information. Under sufficient magnetic field, after 2 pulses, the directional

information will be corrected in uncalibrated mode, as shown in Figure 4-5. When turning left, the pulse length is 90 μ s or 360 μ s.



6-5 Rotation direction indication

Note：Specific signal parameters are shown in Figure 10-1 PWM interface definition (timing characteristics)

7. Output description

7.1 Circuit Description

The circuit is powered by an internal voltage regulator. The on-chip oscillator is used as a clock generator for DSP and output encoder.

7.2 Speed signal circuit:

During the power on phase (uncalibrated mode), the output is disabled (low state). The differential input signal is digitized in a high-speed A/D converter and provided to the DSP part of the circuit. Extract the minimum and maximum values of the input signal and calculate their corresponding arithmetic mean. The offset of the average value is determined and fed into the offset cancellation DAC.

After successfully correcting the offset, enable the output switch.

In operation mode (calibration mode), the DSP's bias correction algorithm switches to low jitter mode, thereby avoiding oscillation of the bias DAC LSB. The switch occurs at zero crossing. It is only affected by the small residual offset of the comparator and the propagation delay time of the signal path, which is mainly determined by the noise limiting filter. Signals below the predefined threshold Δ B limit will not be detected. This can prevent unnecessary switching.

The comparator also detects whether the signal amplitude exceeds ΔBWarning or ΔBEL. This information is fed into the DSP and output encoder. Generate high output current pulse length based on rotational speed, rotation direction, and magnetic field strength.

7.3 Direction signal circuit:

The differential signal between the average values of the third Hall probe and the differential Hall probe pair is obtained by the directional input amplifier. After being digitized by the directional ADC, the signal is sent to the DSP circuit. There, the phase of the signal related to the speed signal is analyzed and the directional information is transmitted to the output encoder.

7.4 Static state:

When the wheel and chip exceed a certain distance or stop rotating, the chip outputs static state information, as shown in Figure 10-2 static protocol, with a pulse length of 1.44ms and a period of 737ms.

8. Absolute limit parameter

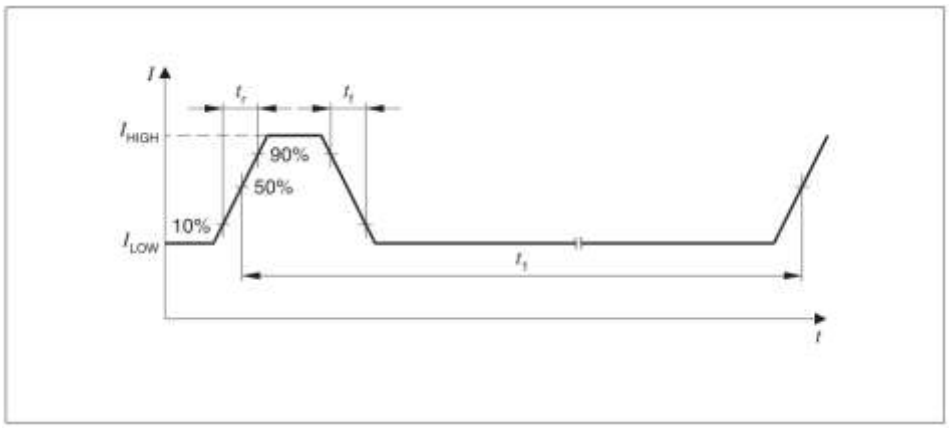
Exceeding the limit parameters during use can lead to unstable chip functionality, and prolonged exposure to this environment can damage the chip. Tj = -40℃ to 150℃, 4.5V≤VDD≤16.5V.

Symbol	Parameter	Min	Max	Unit	Condition
V_{DD}	Power supply Voltage	-0.3		V	Tj<80℃
			16.5	V	Tj=170℃
			20	V	Tj=150℃
			22	V	Tj=150℃ t=10×5min
			24	V	t=10×5min R_M≥75Ωincluded in V_{DD}
			27	V	t=400ms,R_M≥75Ω included in V_{DD}
Urev	Reverse voltage	-22		V	t<1h， R_M≥75Ωincluded in V_{DD}
Irev	Reverse polarity current		200	Ma	External current limitation required, t < 4 h
Tj	Junction temperature	-	150		5000h,V_{DD} <16.5V
		-	160		2500h,V_{DD} <16.5V
		-	170		500h,V_{DD}<16.5V
		-	190		4h,V_{DD} <16.5V

T_A	Operating ambient temperature	-40	150	℃	
V_{ESD}	Antistatic capacity	-	±12	kV	AEC-Q100

9. Electrical characteristic

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Electrical characteristic						
Operating voltage	V_{DD}	4.5	--	20	V	
Operating current (low)	I_{LOW}	5.9	7	8.4	mA	
Working current (high)	I_{HIGH}	11.8	14	16.8	mA	
Working current ratio	I_{HIGH}/I_{LOW}	1.9	2.1	2.3		
Output swing rate	t_r(rise)	8		22	mA/μs	R_M = 75 Ω +/-5% Figure 9-1
	t_f(down)	8		28	mA/μs	R_M = 75 Ω +/-5% Figure 9-1
linearity	dI/dV_{DD}			90	μA/V	
Initial calibration delay	$t_{d,input}$	255	300	345	μs	
Power-on time u	t_{pu}			100	μs	
Duty cycle	DC	40	50	60	%	
Signal frequency	f	1		2500	Hz	
		2500		5000	Hz	
Signal Jitter 1Hz<f<2500Hz	$S_{Jit-close}$			±2	%	1σ value V_{DD}=12 V ΔB ≥ 2 mT
Signal Jitter 2500 Hz < f < 10000 Hz	$S_{Jit-close}$			±3	%	1σ value V_{DD}=12 V ΔB ≥ 2 mT



9-1 Definition of Signal Rise Time tr and Fall Time tf

10. Temporal characteristic

Unless otherwise specified, the following parameters are tested under constant amplitude and bias of the input signal (test conditions are V_{DD}=12V, T_A=25 ℃, circuit reference test circuit diagram 10-1).

Symbol	Parameter	Description	Min	Typ	Max	Unit
$t_{pre-low}$	Pre output low current length	Figure 10-1	38	45	52	μs
t_{LR}	Warning pulse length	Figure 10-1	38	45	52	μs
t_{DR-L}	Pulse length in the left rotation direction	Figure 10-1	76	90	104	μs
t_{DR-R}	Pulse length in the right rotation direction	③Figure 10-1	153	180	207	μs
$t_{DR-L\&EL}$	Left rotation and low magnetic field warning pulse length	Figure 10-1	306	360	414	μs
$t_{DR-R\&EE}$	Right rotation and low magnetic field warning pulse length	④Figure 10-1	616	720	828	μs
f_{ELmax}	Maximum frequency of low magnetic field warning pulse		--	117		Hz
t_{stop}	Static pulse length	⑤Figure 10-2	1.232	1.44	1.656	ms
T_{stop}	quiet period	Figure 10-2	590	737	848	ms

PWM current interface description:

① To achieve reliable internal transmission, a low current tpre low is pre output between the rising edges of the corresponding output pulses for each magnetic change. Follow the signal pulse (high current) output.

② If the magnetic field difference is below ΔB warning, the output pulse length is 45μs. The warning

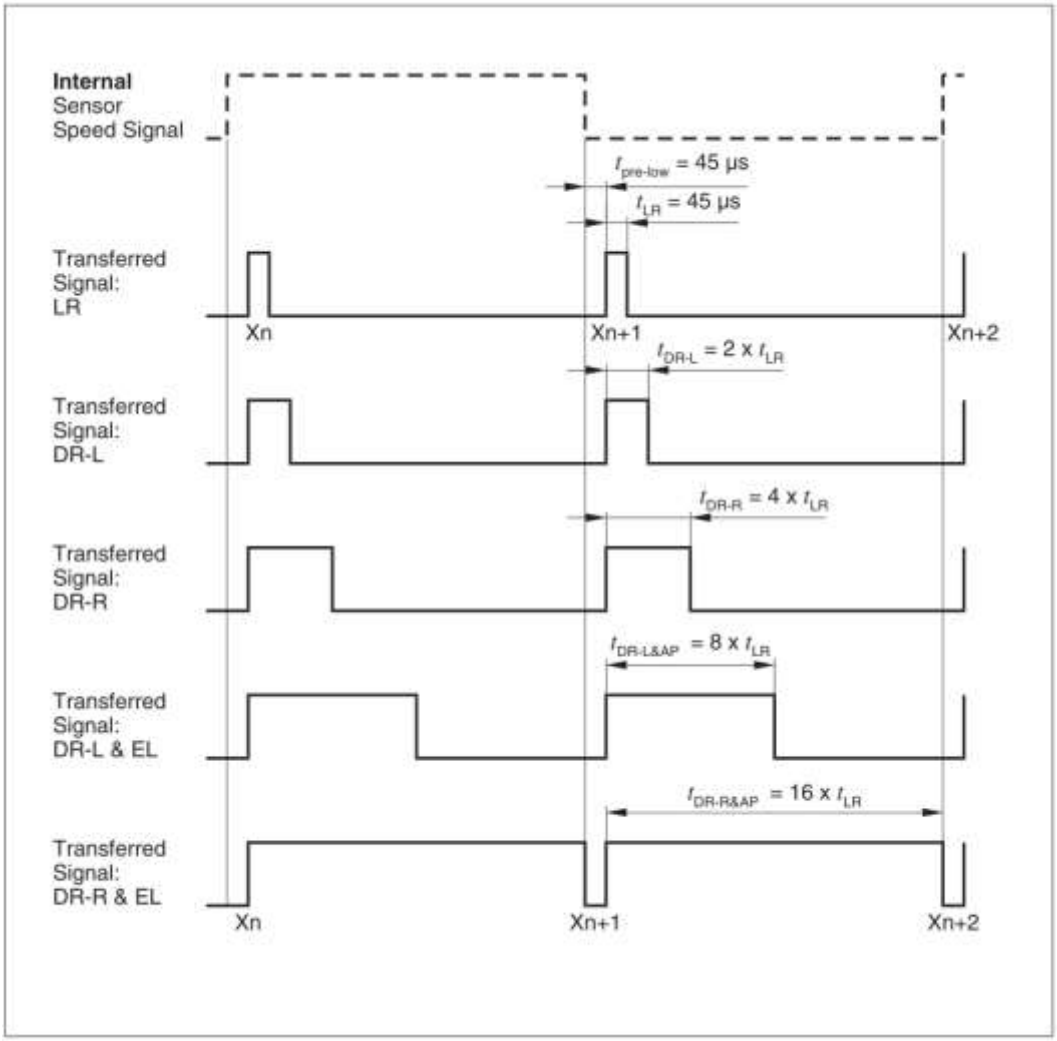
output dominates, which means that the direction and assembly position information close to the limit air gap are disabled.

③ If the magnetic field difference exceeds ΔBEL, the output pulse length will be 90μs or 180μs depending on the rotation direction.

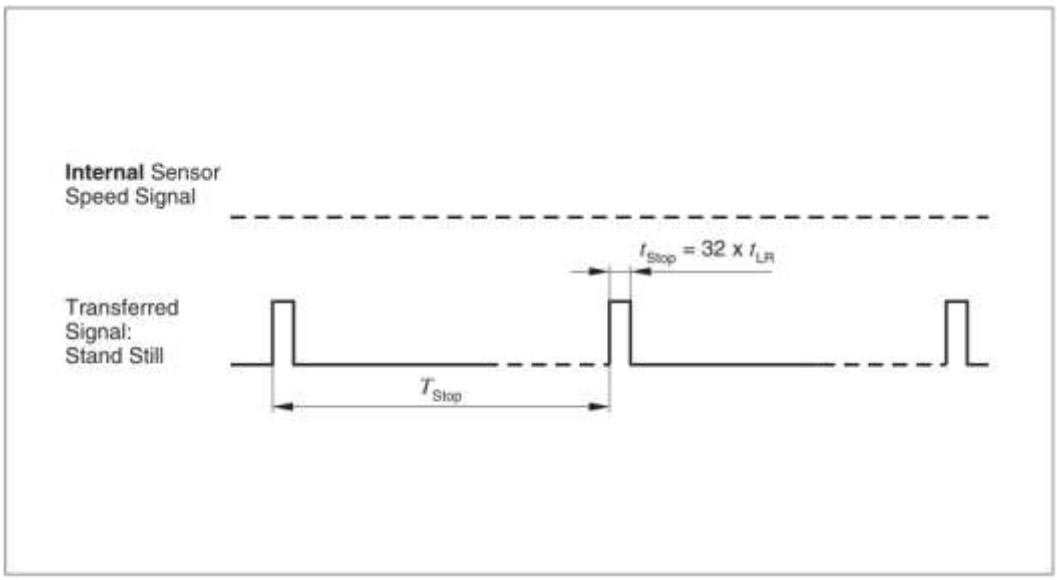
④ When the magnetic field difference is less than ΔBEL, according to left or right rotation, the output pulse lengths are 360μs and 720μs, respectively. Due to the reduced cycle time at higher frequencies, these longer pulses are only output to a frequency of approximately 117Hz. For higher frequencies and differential magnetic fields below Δ BEL, the output pulse lengths are 90μs or 180μs, respectively.

⑤ When the undetected magnetic difference signal exceeds the stationary period Tstop, output a stop pulse. Usually, when the first output stop pulse occurs, the circuit returns to uncalibrated mode.

For magnetic field differences below the ΔB limit, signal loss occurs.



10-1 Schematic diagram of PWM interface definition



10-2 Static Output Protocol

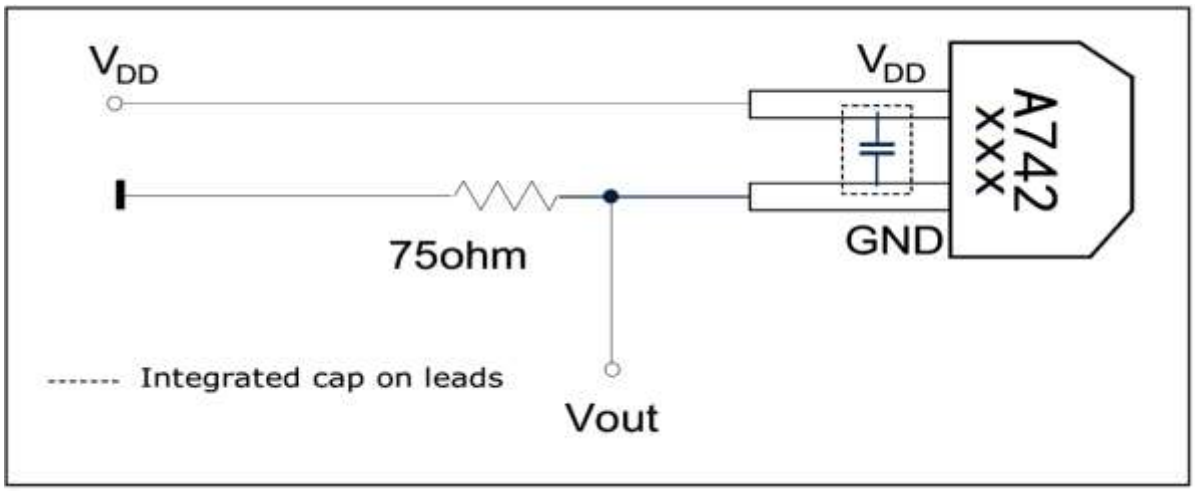
11. Magnetic field characteristic

Unless otherwise specified, the following parameters are tested under constant amplitude and bias of the input signal (test conditions are V_{DD}=12V, T_A=25℃, circuit reference test circuit Figure 11- 1).

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Pre-induction	B_0	-500	-	+500	mT	
Pre-induction offset between outer probes	$\Delta B_{stat., l/r}$	-30		+30	mT	
Differential induction	ΔB	-120		+120	mT	f=1kHz, Bdiff=5mT
Pulse length in the right rotation direction	tDR-R	153	180	207	μs	Figure 10-1
Threshold limit	ΔB_{Limit}	0.35	0.8	1.5	mT	1Hz<f_{mag}<2500Hz
				1.6	mT	2500Hz<f_{mag}<10000 Hz
The difference in the magnetic field required to start	$\Delta B_{startup}$	0.7	1.4	3.3	mT	1Hz<f_{mag}<2500Hz
				3.9	mT	2500Hz<f_{mag}<10000 Hz

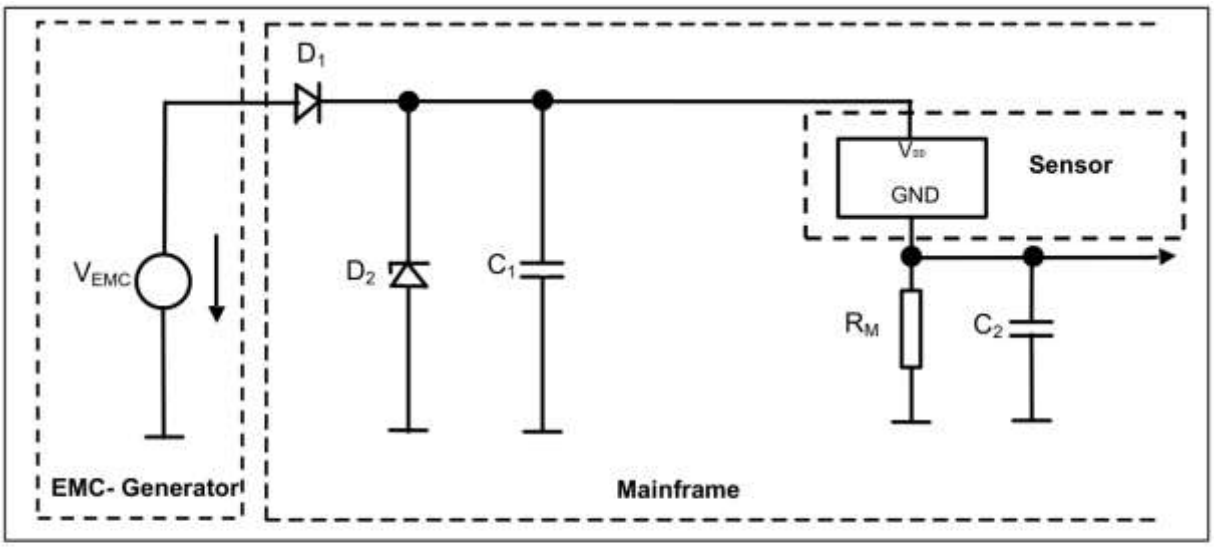
12. Reference circuit

12.1 Test Circuit



12-1 Test Circuit

12.2 Application reference circuit

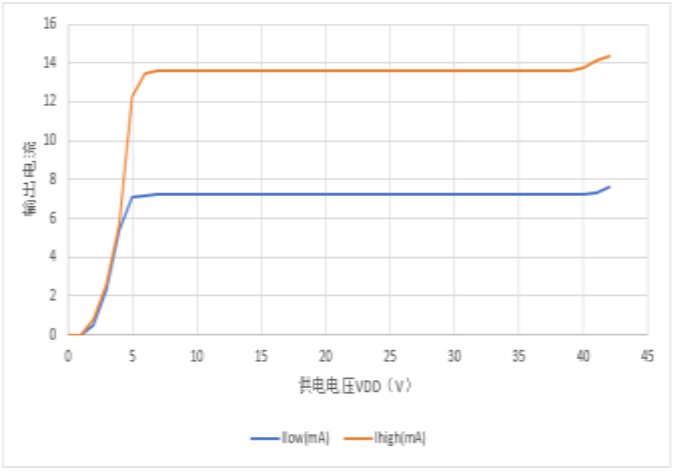


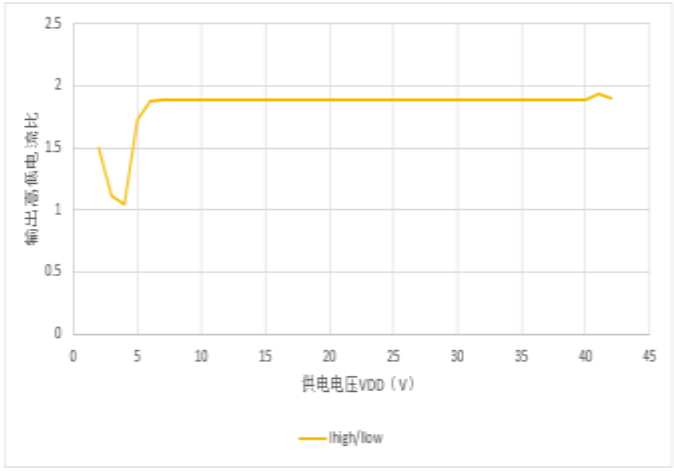
Components:	D1:	1N4007
	D2:	T 5Z27 1J
	C1:	10μF/35V
	C2:	1nF/1000V
	RM:	75Ω/5W

12- 2 Application reference circuit

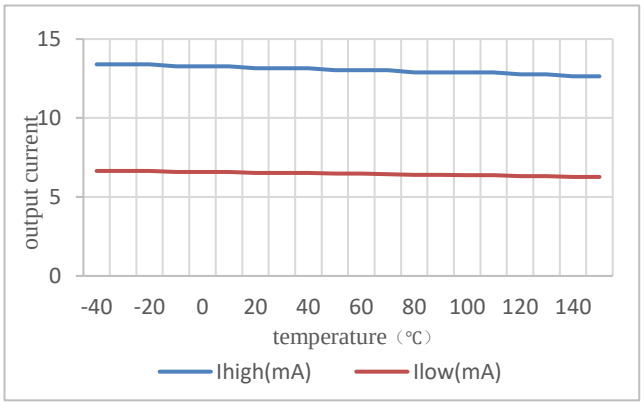
13. Characteristic curve

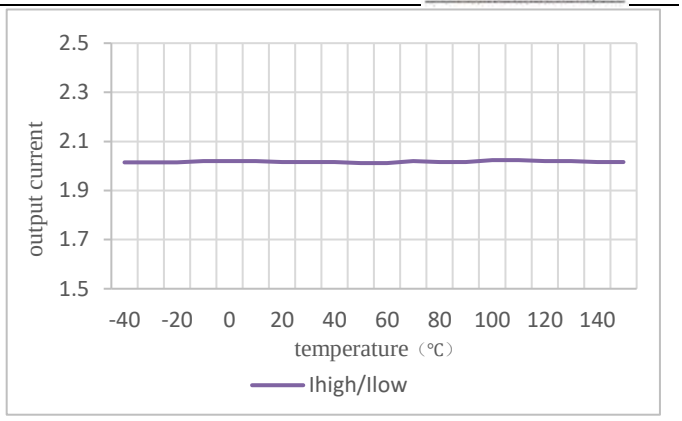
Performance characteristic test (test circuit diagram 12-1)



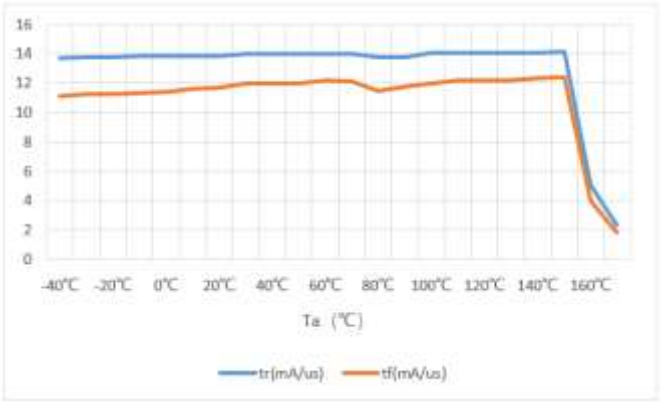


13-1 Working current and current ratio under voltage of 0-42V

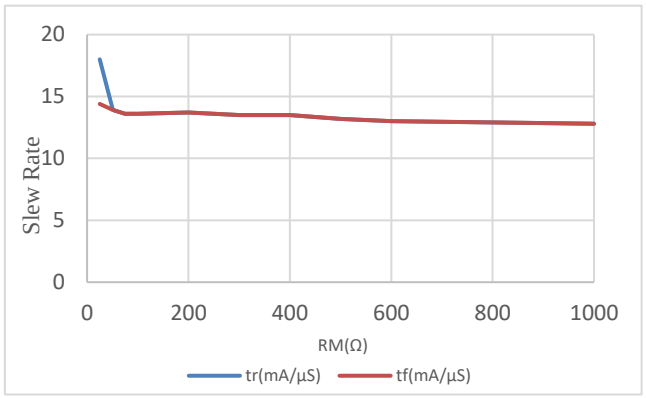




13-2 -40 to +150 °C Operating current and current ratio

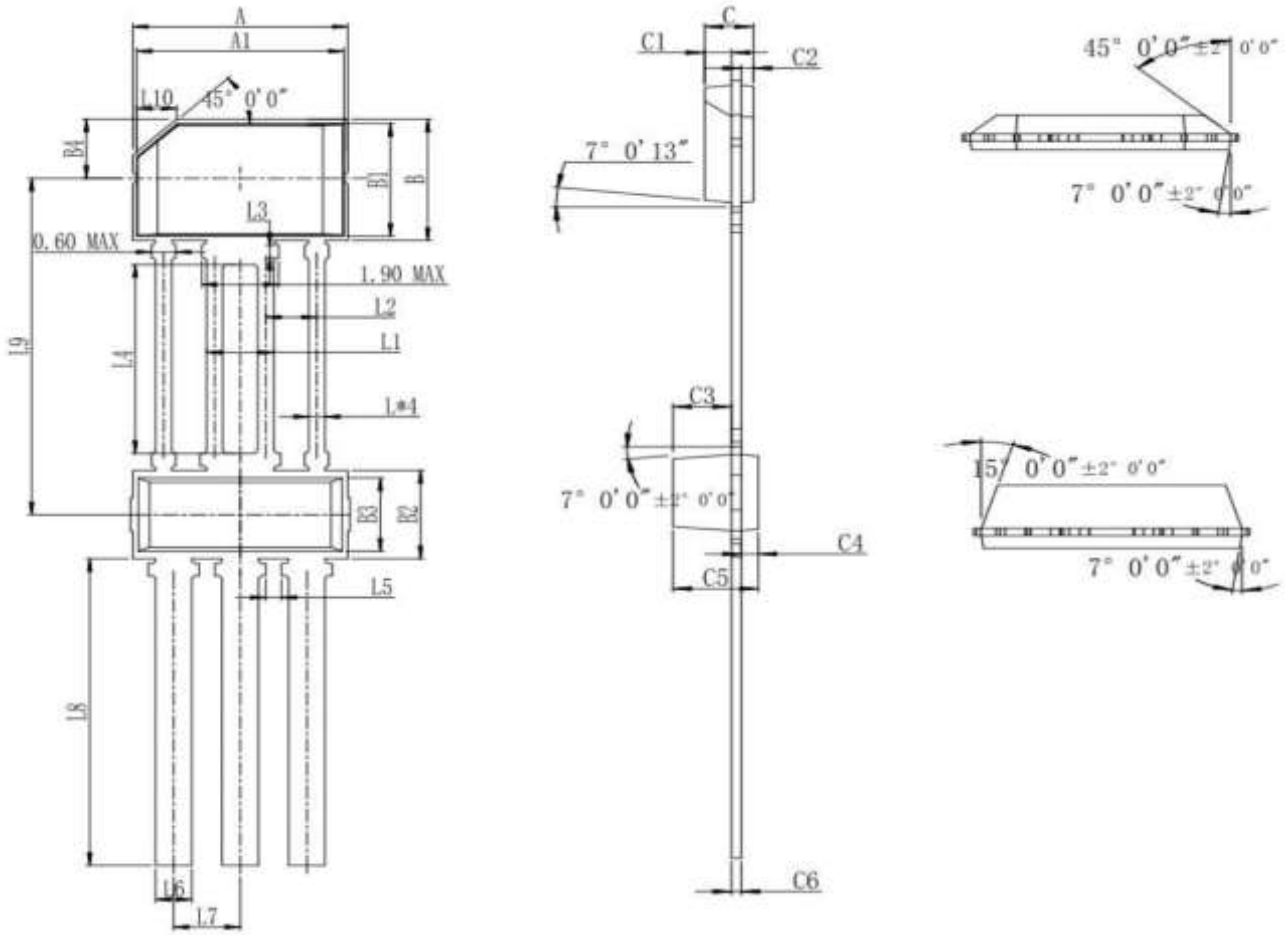


13-3 Output signal slew rate at -40~+150 ℃ temperature



13-4 RM (1~1000) output signal slew rate

14. Package information



15.Note

- Hall chips are sensitive devices, and electrostatic protection measures should be taken during use, installation, and storage.
- During installation and use, mechanical stress applied to the device casing and leads should be minimized as much as possible.
- It is recommended that the welding temperature should not exceed 350 ℃ and the duration should not exceed 5 seconds.
- To ensure the safety and stability of Hall chips, it is not recommended to use them beyond the parameter range for a long time.

16. Historical Version

No.	Time	Describe
1	February.024	Publish
2	April,2024	Update description ambiguity
3	April,2024	Revise the layout